REMARKS

Applicants appreciate the thorough review of the present application that is reflected in the Office Action mailed August 1, 2006. For the reasons discussed below, Applicants respectfully submit that the present application, as amended herein, is now in condition for allowance.

I. The Claim Amendments

Applicants have amended Claim 1 to stress various of the differences between the cited references and the inventions of the pending claims. Applicants have amended dependent Claims 2-16 to correct the preamble of each claim in light of the amendments to Claim 1. Applicants have amended Claim 4 to address the informality noted in the Office Action. Applicants have amended Claims 9 and 12 to remove the "second bit line" recitation. Applicants have amended Claim 15 to correct a typographical error in the claim dependency. Applicants have also amended the claims to delete the phrase "self-aligned."

Applicants have also cancelled Claims 41 and 42, thereby obviating the objection to the drawings. Applicants have cancelled non-elected Claims 17-40. Finally, Applicants have added new Claims 43-46, which are drawn to the elected species.

II. Amended Claim 1 is Patentable Over the Cited Art

Claim 1 stands rejected as anticipated under 35 U.S.C. § 102(b) by U.S. Patent Application Publication No. 2002/0060332 A1 to Ikeda et al. ("Ikeda"). Alternatively, Claim 1 stands rejected as obvious under 35 U.S.C. § 103 over Ikeda in view of U.S. Patent No. 5,625,591 to Kato et al. ("Kato"). Applicants respectfully traverse these rejections for the following reasons:

A. The Cited Art Does Not Disclose the Recited First Contact Pad

As amended, Claim 1 recites:

1. A semiconductor device, comprising:

(a) a test pattern that includes

a word line on a semiconductor substrate;

an active region comprising a first impurity doped region and a second impurity doped region;

a first contact pad electrically connected to the first impurity doped region**, the first contact pad having a first region that covers the first impurity doped region and a second region that is offset from the first impurity doped region**;

a first bit line electrically connected to the first contact pad;

a second contact pad electrically connected to the second impurity doped region;

a second conductive line electrically connected to the second contact pad; and

(b) a first probing pad electrically connected to the first bit line; and

(c) a second probing pad electrically connected to the second conductive line.

(Emphasis added). The Office Action states that contact hole 27 of Ikeda comprises the "first . . . contact pad" of Claim 1, and that the data line DL comprises the "first bit line" of Claim 1. (Office Action at 3-4). Applicants respectfully submit, however, that **Ikeda does not teach or disclose providing a first contact pad that has "a first region that covers the first impurity doped region and a second region that is offset from the first impurity doped region"** as recited in amended Claim 1. Instead, Ikeda only shows contact hole 27 having a region directly over source/drain region 20. Moreover, there would be no reason to modify the device of Ikeda to have a first contact pad that includes the first and second regions recited in amended Claim 1. Accordingly, the rejection of Claim 1 should be withdrawn for this reason.

B. Ikeda Does Not Disclose a Semiconductor Test Pattern

Claim 1 has also been amended to expressly recite in the body of the claim that the word line, the first bit line and various other components are part of a "test pattern." As explained in the specification of the present application, "semiconductor device test patterns may be used to measure operational properties of a semiconductor device" such as, for example, operational properties of a cell transistor in a DRAM memory device (Specification at p. 2, lines 25-29). In contrast, the cited portion of Ikeda discloses a flash memory device as opposed to a test pattern. Moreover, while the secondary Kato reference includes a "source bias circuit" 201 that has a "source bias test pad" 202 that may be used to measure the threshold voltage of the memory cells, Kato does not teach or disclose providing a test pattern

that includes each of (1) a word line, (2) an active region, (3) a first contact pad, (4) a first bit line, (5) a second contact pad and (6) a second conductive line as recited in amended Claim 1. As such, neither, Ikeda, Kato, nor the combination thereof suggest the particular test pattern of amended Claim 1 and, as such, the rejection of Claim 1 should be withdrawn for this additional reason.

III. The Rejections of Claims 2-7 and 9

Claims 2-7 and 9 each depend from Claim 1 and hence are patentable for each of the reasons, discussed above, that Claim 1 is patentable over the cited art. In addition, Applicants respectfully submit that at least Claims 2 and 5-6 are independently patentable over the cited art.

In particular, as amended, Claim 2 further recites that the device includes (1) "a first contact plug that penetrates a first insulation layer between the first contact pad and the first bit line, the first contact plug electrically connecting the first contact pad to the first bit line" and (2) "a second contact plug that penetrates the first insulation layer, the second contact plug electrically connecting the second contact pad to the second conductive line." In contrast, in the device of Ikeda, the identified first contact pad (contact hole 27) is directly connected to a first of the data lines DL and the identified second contact pad (contact hole 28) is directly connected to a second of the data lines DL. (Ikeda at Fig. 4; see also Office Action at 5). Thus, Ikeda does not teach or disclose, providing either the "first contact plug" or the "second contact plug" of Claim 2, and therefore does not anticipate Claim 2.

Claim 5 recites that the semiconductor device further includes "a third contact plug between the first bit line and the first probing pad that electrically connects the first bit line and the first probing pad." Claim 6 similarly recites that the semiconductor device further includes "a fourth contact plug between the second conductive line and the second probing pad that electrically connects the second conductive line and the second probing pad." The Office Action states that it is "inherent" that some sort of contact is provided between the bit line and the first probing pad and between the second conductive line and the second probing pad. (Office Action at 5). However, it clearly is not "necessarily" the case that the device of Ikeda would include a contact plug between each "inherently" present probing pad and the

line that such probing pads are allegedly electrically connected to. Instead, each probing pad (if they in fact existed) could clearly be directly connected to the respective lines. As such, the Office Action has not and cannot show that Ikeda necessarily discloses the recitations of Claims 5 and 6. This provides an independent basis for withdrawal of the rejections of Claims 5 and 6.

IV. New Claims 43-46

Applicants have added new Claims 43-46, each of which are drawn to the elected species. New Claim 43 recites that the "first bit line is laterally offset from the first and second impurity doped regions." In contrast, as shown in Fig. 4 of Ikeda, the data line DL is directly over each of the source/drain regions 20. Accordingly, Claim 43 is also independently patentable over Ikeda.

New Claims 44 and 45 recite that the device further includes a second insulating layer between "the first bit line and the first probing pad" and between "the second conductive line and the second probing pad", respectively, and that the third and fourth contact plugs "penetrate the insulating layer." Ikeda does not disclose any such second insulating layer, nor does Ikeda disclose third or fourth contact plugs that penetrate such an insulating layer. Accordingly, Claims 44 and 45 are also independently patentable over Ikeda.

Finally, Claim 46 recites that "the first bit line is over the second region of the first contact pad." The alleged "first contact pads" in Ikeda do not have such first and second regions, nor is the data line DL of Ikeda over any such second region of the identified "first contact pad." Accordingly, Claim 46 is also independently patentable over Ikeda.

V. The Withdrawal of Claims 8 and 10-16

Claims 8 and 10-16 were not examined as being directed to a non-elected species, with no generic claim having been indicated as allowable. However, as noted in Applicants prior response, at least Claims 1-6 are generic claims. As discussed above, each of these generic claims is patentable over the cited art. Accordingly, Applicants also respectfully submit that examination and allowance of Claims 8 and 10-16 is also appropriate.

VI. Conclusion

For the foregoing reasons, Applicants respectfully submit that Claims 1-16 and 43-46 are now in condition for allowance.

Respectfully submitted,

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